# **SPIBPro**



## SPISim Environment Overview:

With the ever increasing fast data rate in today's system design, a growing percentage of products suffer from signal degradation. Noises such as over/undershoot, ringing, jitter and incorrect setup-hold time caused by impedance/length mismatching may not only decrease the data transmission rate, but also cause system to fail.

Conventionally, hardware engineers and signal integrity specialists alike relies on multiple tools (e.g. solvers, matlab like scripting environments or customized tools) to analyze these signaling issues. While most of the users only utilize very small portion of these tools' capabilities, yet they spend lots of resources (e.g. licensing cost and engineering efforts) to acquire the capabilities and be familiar with the tool usage.

SPISim's products integrates most frequently used signal/power analysis capabilities in a single easy-to-use environment at very reasonable cost. It is to serve most SI/PI engineers' daily tasks' needs and minimize underutilized tool cost.

SPIBPro is one of SPIPro's module focusing on IBIS modeling and analysis. See SPIPro's product datasheet for other modules' capabilities.

### **APPLICATION SCOPES:**

- IBIS model data visualization, inspection, generation and optimization.
- Full IBIS modeling flow for all model types including differential and series.
- IBIS model figure of merits (FOM) reporting and performance extraction.
- Support from IBIS V3.2 (signal only) to IBIS V5.1 (power aware) model gener-

## MAJOR BENEFITS:

- Single integrated environment with all others SPISim's products (e.g. VPro for waveform viewing and analysis), straight-forward UI.
- Support IBIS model generation from either scratch or existing simulation data. From V3.2 ~ V5.1 are supported.
- Best-known-method based flow for buffer stimulation, simulation, model generation, syntax check, validation and reporting.
- Tuning capability to generate overclockable buffer. Optimization process select best data point to generate accurate yet compact model. Auto fix for DC-mismatch issue and DC trimming.
- Intuitive model inspector to visualize modeling data and cross reference its texture data. Edit curve with simple mouse drag.





## DATASHEET P2/2

## **SPIBPro**

#### **IBIS Model Inspection & Visualization:**

SPIBPro can import IBIS model to cross check texture data and its associated VT/IV/IT data curves. Drop-down menu allow simple switching between different TYP/MIN/MAX corners and VCC/VSS related curves. Convenient in-place data editor allow users to update data point value easily with mouse drag. Multi-pane data viewing allow comparison of IT and VT on the same time axis yet with appropriate voltage/current Y-axis scale.

## IBIS Modeling from Begin to End:

SPIBPro is an add-on flow on SPIMPro for IBIS model inspection, generation, validation and reporting. It can generate IBIS model from either transistor buffer sub-circuit and terminals settings provided or existing buffer simulation results. Stepby-step based full flow will guide user from generate HSpice\* compatible input files for test-bench simulations, extract results to generate IBIS models, exercise golden parser to check the syntax/ values, and correlate the results to original transistor buffer by validating generated IBIS models and analyze their electrical parameters qualitatively. SPIBPro supports from V3.2 (signal only) to V5.1 (power aware) model generation. It also has fine tuning capability to generate overclockable buffer without sacrificing modeling accuracy. Smart "bestpoint selection" algorithm to choose best 100 or 1000 data points to enable generated model compact yet accurate.

## **IBIS Modeling Utility Functions:**

Include trimming dc data, auto-fixing dc mismatches of existing models, best N-point selection for data, test-bench set-up for test data. Header generation for model selectors are all available.



\* SPISim LLC is a member of Synopsys HSPICE Integrator Program. For more info. About HSpice, please visit www.synopsys.com.

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